REMARKS

The application includes claims 2-5, 7-9, 11-19, and 22-49 prior to entering this amendment.

The examiner rejects claims 2-5, 7-9, 11-19, and 22-49.

The applicant amends claims 2, 4, 5, 7, 13, 17, 19, 22, 24-27, 31, 32, 36, 39, 44, 47, and 49. The application remains with claims 2-5, 7-9, 11-19, and 22-49 after entering this amendment.

The applicant adds no new matter and requests reconsideration.

Claim Rejections - 35 U.S.C. § 102

The examiner rejects claims 44-46 and 49 under 35 U.S.C. § 102(e) as being anticipated by Grisamore (U.S. Patent 6,535,901). The applicant traverses the rejections.

Regarding claim 44, the claim recites "the summing module…comprises… a hybrid Wallace tree comprising one or more elements, wherein the elements comprise one or more adders having one or more associated registers and one or more additional registers." Grisamore does not teach a summing module comprising adders with associated registers and additional registers. The Office Action proposes that Grisamore teaches this feature at "col. 1 lines 32-42" because it teaches "appropriate registers at optimal points in each adder for pipelining." See Office Action page 3. However, the cited portion of Grisamore actually teaches that *a multiplier* may have registers at optimal points; not a summing module. This is made clear by the cited portion where it specifically states "[s]uch an architecture provides the advantages of efficiency in integrated circuit lay out and ease of pipelining by using registers *at optimal points in the array multiplier.*" See Grisamore col. 1, lines 36-38 (emphasis added). Consequently, Grisamore does not teach a summing module comprising adders with associated registers and additional registers.

Further, even if the proposition made by the Office Action were to be accepted, it still would not anticipate the claim. For instance, the Office Action proposes that Grisamore teaches "appropriate registers at optimal points in each adder for pipelining." See Office Action page 3. Even taking this as true and supposing that these 'appropriate registers' could be considered to

anticipate the 'associated registers' recited in the claim, Grisamore still does not teach any element that could anticipate the 'additional registers' recited in the claim.

Finally, claim 44 recites "an integrated multi-input adder." The Office Action proposes that Grisamore teaches "a multi-input adder (e.g. adder 18 in Figure 1)." See Office Action page 3. The applicant agrees with the Office Action that Grisamore teaches an adder 18 in Figure 1, but this is not what the claim recites. The claim specifically recites an *integrated* multi-input adder. The applicant submits that the adder 18 of Grisamore is not integrated, as that term is defined by the present application. MPEP 2111.01(IV) states that "[w]here an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim." At page 6, lines 14-18 of the present application, the applicant specifically defined 'integrated' to mean that accumulator bits are introduced into registers in the summing module. Grisamore does not teach that accumulator bits are introduced into registers in the summing module, at least because, as described above, Grisamore does not teach any registers in its summing module. Therefore, the adder 18 of Grisamore is not an integrated adder and cannot anticipate the integrated multi-input adder recited in the claim.

The Office Action argues that the adder 18 of Grisamore is integrated because the "technical definition" of 'integrated' means it is "implemented or manufactured as a single compact unit." See Office Action page 14. Setting aside the validity of this definition in general, this definition is inconsistent with the definition provided in the specification, as cited above. MPEP 2111.01(I) states that "the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification." In the Response to Arguments, the meaning supplied by the Office Action is inconsistent with the specification and therefore the claim should not be examined using this definition.

Also, the applicant would like to point out that even using the definition provided by the Office Action; the claim is still not anticipated. For instance, the Office Action argues that the technical definition provided does not require the adder 18 of Grisamore to be integrated with the reduction tree module 14. However, claim 44 specifically recites "the summing module, as configured, comprises: a hybrid Wallace tree...and an integrated multi-input adder." Therefore, using the equivalences and the definition of 'integrated' proposed by the Office Action, Grisamore does have to teach that the adder 18 and the reduction tree module 14 are

implemented or manufactured as a single compact unit in order to anticipate the claim. Grisamore does not teach this.

For at least the reasons identified above, Grisamore fails to anticipate claim 44 because it does not teach each and every element recited in the claim. MPEP § 2131.

Claims 45, 46, and 49 depend from claim 44 and inherently contain the features of claim 44. Consequently, Grisamore fails to anticipate claims 45, 46, and 49 for at least the same reasons it fails to anticipate claim 44.

Further regarding claim 46, the Examiner rejects claim 46 under 35 U.S.C. 102(e) as being anticipated by Grisamore by stating "[r]e claim 46, it is an apparatus claim of claim 3. Thus, claim 46 is also rejected under the same rationale as cited in the rejection of claim 3." See Office Action page 3. However, claim 3 is not rejected under 35 U.S.C. 102(e) as being anticipated by Grisamore. Claim 3 is rejected "under 35 U.S.C. 103(a) as being obvious over Grisamore in view of Chang." See Office Action page 4. Consequently, claim 3 could not have provided the same rationale for the rejection of claim 46 because claim 46 is rejected under 35 U.S.C. 102(e) and claim 3 is rejected under 35 U.S.C. 103(a). The applicant submits that claim 46 is not anticipated by Grisamore and is allowable as previously presented.

Claim Rejections - 35 U.S.C. § 103

The examiner rejects claims 2-5, 7-9, 11-12, 17-19, 22-27, and 47-48 under 35 U.S.C. § 103(a) as being unpatentable over Grisamore in view of Chang et al. ("Hardware-Efficient Implementations for Discrete Function Transforms Using LUT-Based FGPAs"). The applicant traverses the rejections.

Regarding claim 2, the claim recites "a summing module generator coupled with the dedicated logic device, wherein the summing module generator is adapted to structure the dedicated logic device to implement a multi-stage summing module." The Office Action proposes that partial product generator 12 of Grisamore is the recited dedicated logic device and that reduction tree module 14 and memory 16 are the recited summing module generator. See Office Action page 4. However, Grisamore does not teach that the reduction tree module 14 and memory 16 of Grisamore are adapted to structure partial product generator 12 to implement a multi-stage summing module. The Office Action does not point to any specific teachings in Grisamore that teach this feature, and the applicant finds no such teachings. Such a teaching

would be contrary to the disclosure of Grisamore because Grisamore does not teach that its partial product generator 12 is structured into a summing module; it specifically teaches that the partial product generator 12 is used to generate partial products. See Grisamore column 2, lines 55-56. Therefore, the partial product generator 12 of Grisamore cannot be equivalent to the recited dedicated logic device. Further, Grisamore specifically teaches that processing module 72 of FIG. 8 develops the fast multiply accumulator in accordance with the method of FIG. 9. See Grisamore col. 7, lines 10-29. However, Grisamore does not teach that processing module 72 is coupled to a dedicated logic device and therefore the processing module 72 cannot be equivalent to the recited summing module generator. Consequently, Grisamore does not contain an equivalent element to either the recited summing module generator or the dedicated logic device.

Claim 2 further recites "a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers." As described above with respect to claim 44, Grisamore does not teach associated registers and single registers in a summing module. Besides the arguments presented above with respect to claim 44, the Office Action also proposes that Grisamore teaches "appropriate registers at optimal points in each adder...inherently." See Office Action page 4. "When relying on the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art." MPEP 2112(IV), *citing* Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter., 1990), emphasis in original. "Furthermore, the fact that a certain result may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." MPEP 2112(IV), *citing* In re Rijckaert, 9 F.3d 1531, 1534 (Fed. Cir. 1993). The Office Action has not provided any basis to support the notion that registers are necessarily associated with each of Grisamore's adders and that single registers are also necessarily included in its reduction tree module 14. As an example, Grisamore specifically teaches that its reduction tree module 14 is directly coupled to memory 16 to store the output of its adders. Since, the outputs of the adders in Grisamore are stored in memory 16; the inclusion of registers in reduction tree module 14 is not necessary in Grisamore. Therefore, a summing module comprising associated registers and single registers is neither explicitly taught in Grisamore nor inherent in Grisamore.

Claim 2 further recites "the summing module is adapted to produce intermediate summation results by combining the multiple input terms." The Office Action identified "1st current multiplicand 20 and 2nd current multiplicand 22 in Figure 1" as the recited multiple input terms. See Office Action page 4. However, elements 20 and 22 of Grisamore do not provide inputs into the reduction tree module 14 (the recited summing module, according to the Office Action); elements 20 and 22 are inputs into partial product generator 12. Consequently, the reduction tree module 14 of Grisamore cannot be adapted to produce intermediate summation results by combining 1st current multiplicand 20 and 2nd current multiplicand 22 because it never receives these as inputs. The Office Action proposes that Grisamore teaches this feature because it teaches "intermediate summation results (e.g. output of reduction tree module 14 as 1st preceding resultant 26 and 2nd preceding resultant 28) by combining the multiple input terms (e.g. partial product terms from generator 12)." However, there are two problems with this proposition. First, elements 26 and 28 of Grisamore are inputs to the reduction tree module 14; not outputs (the applicant submits that in order to produce intermediate summation results, a summing module must output the results, not take them as inputs). Second, the Office Action previously identified 1st current multiplicand 20 and 2nd current multiplicand 22 as the multiple input terms, but now the Office Action is proposing that the plurality of current partial products 24 are the recited multiple input terms. If the plurality of current partial products 24 were to be considered equivalent to the recited multiple input terms, rather than elements 20 and 22, it would be even more clear that the rejections of previous portions of the claim are not valid because the structural relationships recited in the claim would not be met by Grisamore. Consequently, Grisamore does not teach a summing module adapted to produce intermediate summation results by combining the multiple input terms, as recited in claim 2.

Claim 2 also recites "the summing module generator is further adapted to implement an integrated multi-input adder into the summing module." As described above with respect to claim 44, Grisamore does not teach an *integrated* multi-input adder, as that term is defined in the present application. Further, claim 2 specifically refers to implementing the adder *into* the summing module. The adder 18 of Grisamore is not implemented *into* the reduction tree module 14. See Grisamore FIG. 1. Therefore, even setting aside the issue of the definition of 'integrated', Grisamore still does not teach an adder equivalent to the recited integrated multi-

input adder because Grisamore specifically teaches that the adder 18 and the reduction tree module 14 are separate components.

Claim 2 further recites "wherein the integrated multi-input adder includes a plurality of inputs, wherein at least a portion of the plurality of inputs are adapted to receive feedback input of accumulator bits from one or more of the full-adders and associated registers, half-adders and associated registers, and single registers of the summing module." The Office Action proposes that "feedback from memory 16 in Figure 1" is the recited feedback input of accumulator bits. See Office Action page 5. However, as shown in Figure 1 of Grisamore, the feedback from memory 16 (1st preceding resultant 26 and 2nd preceding resultant 28) do not provide inputs into adder 18. As indicated by the arrows in Figure 1, elements 26 and 28 are directed away from the inputs to adder 18 and actually provide inputs to reduction tree module 14. See Grisamore FIG. 1. Finally, Grisamore does not teach that elements 26 and 28 are accumulator bits from one or more of the full-adders and associated registers, half-adders and associated registers, and single registers of the summing module, as recited in the claim. This is so at least because Grisamore does not teach that its reduction tree module 14 includes any associated or single registers. Therefore, Grisamore does not teach an integrated multi-input adder including a plurality of inputs, some of which receive feedback, as recited in claim 2.

Claim 2 also recites "the integrated multi-input adder is further adapted to produce a final sum of the multiple input terms by combining the intermediate summation results." The Office Action proposes that Grisamore teaches this feature because it teaches a multiplied accumulated resultant 34 combining the outputs of 14. See Office Action page 5. However, as discussed above, Grisamore does not teach an adder implemented in the reduction tree module 14. Instead, Grisamore teaches that the adder 18 is separate from the reduction tree module 14. Therefore, Grisamore could not teach an integrated multi-input adder in a summing module adapted to produce a final sum of the multiple input terms by combining intermediate summation results, as recited in the claim.

Chang is merely cited for the proposition that partial product generator 12 of Grisamore could be a dedicated logic device and therefore Chang does not remedy the deficiencies of Grisamore identified above.

The Office Action acknowledges that Grisamore does not teach a dedicated logic device as recited in claim 2. However, the Office Action proposes that Chang teaches "the series of

Boolean function generators as a summing module is coupled with a dedicated logic device comprising a FPGA (e.g. 2nd paragraph on the left column page 309)." See Office Action page 5. To the contrary, Chang actually teaches an FPGA programmed to implement a summing module; not an FPGA coupled to a summing module. See Chang Section 1. Further, claim 2 specifically recites "a summing module *generator* coupled with the dedicated logic device." Therefore, even if Chang did teach what the Office Action proposes, it still would not result in the claimed invention because it would teach a summing module coupled to an FPGA, not a summing module generator coupled to an FPGA. Therefore, the combination of Grisamore and Chang does not result in the claimed invention.

For at least the reasons identified above, claim 2 is allowable over the combination of Grisamore and Chang because the combination does not teach or suggest all of the features of the claim. MPEP § 2143.

Claims 3-5, 7-9, and 11-12 depend from claim 2, and inherently contain the features of claim 2. Consequently, claims 3-5, 7-9, and 11-12 are allowable over the combination of Grisamore and Chang at least because any claim that depends from a nonobvious independent claim is also nonobvious.

Further regarding claim 3, the claim recites "the multiple input terms include one or more accumulator bits." The Office Action proposes that Grisamore teaches this feature because it teaches elements "26 and 28 wherein each of these bits is the resultant bit of previous or preceding summations." See Office Action page 5. However, the Office Action has already proposed that elements 20 and 22 of Grisamore are the recited multiple input terms. See Office Action page 4. Elements 20 and 22 of Grisamore do not include elements 26 and 28. Therefore, even if elements 26 and 28 were to be considered accumulator bits, they are not included in elements 20 and 22, and so could not be equivalent to the accumulator bits recited in the claim. If elements 26 and 28 were to be considered equivalent to the recited multiple input terms, rather than elements 20 and 22, it would be even more clear that the rejections of claim 2, from which claim 3 depends, are not valid because the structural relationships recited in the claim would not be met by Grisamore. For at least this additional reason, claim 3 is allowable over the combination of Grisamore and Chang.

Further regarding claim 5, the claim recites "each Boolean function generator pairs with an associated register to form an atomic structure of a dedicated logic device." The Office

Action proposes that Grisamore teaches this feature at "col. 1 lines 32-42 wherein appropriate registers at optimal point in each adder for pipelining and col. 1, lines 36-38." See Office Action page 6. However, the cited portion of Grisamore does not teach anything about Boolean function generator pairs having associated registers forming an atomic structure of a dedicated logic device. The Office Action previously acknowledged that Grisamore does not teach a dedicated logic device. See Office Action page 5. If Grisamore does not teach a dedicated logic device at all, as the Office Action acknowledges, it certainly cannot teach Boolean function generator pairs with an associated register to form an atomic structure of a dedicated logic device, as recited in the claim. For at least this additional reason, claim 5 is allowable over the combination of Grisamore and Chang.

Further regarding claim 7, the claim recites "the multi-input adder comprises an adder with an input for each single register in a final stage of the summing module." The Office Action proposes that Grisamore teaches this feature because it shows in FIG. 5 that successive stages of bits are added. See Office Action page 6. However, there is nothing in FIG. 5 of Grisamore, or anywhere else in its disclosure, that teaches an adder with *an input for each single register* in a final stage. Specifically, as described above with respect to claim 44, Grisamore does not teach single registers, so it could not teach an adder with an input for each single register. Further, even if Grisamore did teach registers in general, as the Office Action proposes, this teaching would still not be equivalent to the recited structural relationship recited in claim 7, which specifically refers to an input for each single register. For at least this additional reason, claim 7 is allowable over the combination of Grisamore and Chang.

Further regarding claim 8, the claim recites "the integrated multi-input adder includes a plurality of single registers to receive feedback accumulator bits from the multi-input adder." The Office Action has not pointed to any elements of Grisamore that are considered to be equivalent to the recited plurality of single registers and the applicant finds no such elements. The Office Action does propose that elements 26 and 28 of Grisamore are the recited feedback accumulator bits. See Office Action page 6. However, the Office Action has previously proposed that the adder 18 is equivalent to the recited multi-input adder. See Office Action page 4. In order to meet the claim features, using the propositions in the Office Action, Grisamore would have to teach that elements 26 and 28 are outputs from the adder 18. Grisamore does not teach this. Grisamore specifically teaches that elements 26 and 28 are outputs from memory 16,

not adder 18. See Grisamore FIG. 1. Adder 18 has only one output (multiplied accumulated resultant 34) and this output does not provide any feedback. See id. Therefore, Grisamore does not teach the integrated multi-input adder as recited in claim 8. For at least this additional reason, claim 8 is allowable over the combination of Grisamore and Chang.

Further regarding claim 9, the claim recites "an accumulator coupled with the multi-input adder to feed the accumulator bits back into the summing module." The Office Action has not identified any elements of Grisamore that are considered to be equivalent to the recited accumulator and the applicant finds no such elements. The Office Action proposes that Grisamore teaches this feature because it teaches "feedback from output of 16 to input of reduction tree module 14 in Figure 1." See Office Action page 7. But the Office Action previously identified elements 14 and 16 of Grisamore to be equivalent to the recited summing module generator. See Office Action page 4. The claims do not refer to the summing module generator including the accumulator, and so the memory 16 of Grisamore cannot be the recited accumulator. Therefore, Grisamore does not teach an accumulator as recited in claim 9. For at least this additional reason, claim 9 is allowable over the combination of Grisamore and Chang.

Further regarding claim 12, the claim recites "the dedicated logic device comprises a device with control logic and a block of dedicated logic." The Office Action acknowledges that Grisamore does not teach this feature, but proposes that Chang teaches this feature because it teaches "control signals for controlling the block of hardware." See Office Action page 7. The applicant does not find any teachings in Chang concerning the cited 'control signals'. However, even if Chang did teach 'control signals', such a teaching would still not meet the claim features. The claim specifically recites control logic and a block of dedicated logic; not 'control signals'. Therefore, Chang does not teach control logic and a block of dedicated logic as recited in claim 12. For at least this additional reason, claim 12 is allowable over the combination of Grisamore and Chang.

Regarding claim 17, the Examiner rejects claim 17 as follows: "[r]e claim 17, it is a method claim of claim 2. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 2." See Office Action page 7. However, claim 17 is not just a method claim of claim 2. Claim 17 recites numerous features that were not recited in claim 2 and for which no grounds of rejection were provided in claim 2. For example, claim 17 recites: "forming a summation pattern by which to reduce the terms by partitioning bits of equal significance into

groups of three, remaining bits of equal significance into groups of two, and remaining bits left singly" and "the summing module generator adapted to structure atomic elements of a dedicated logic device to implement a multi-stage summing module." Neither of these features was recited in claim 2, and thus no grounds of rejection were supplied for these features in the rejection of claim 2. Therefore, the final Office Action does not identify any grounds of rejection for these features of claim 17 and the applicant does not find any proper grounds of rejection for these features in the cited references.

Further, claim 17 recites several features that are not taught in Grisamore, Chang, or any possible combination of the two. For example, claim 17 recites "a multi-stage summing module comprising one or more full-adders and associated registers, half-adders and associated registers, and single registers," "an integrated multi-input adder [implemented] into the summing module," and "a final sum of the input terms [produced] by combining the feedback input with the multi-input adder." The combination of Grisamore and Chang does not teach these features, at least for the reasons identified above with respect to claims 2 and 44.

For at least the reasons identified above, claim 17 is allowable over the combination of Grisamore and Chang because the combination does not teach or suggest all of the features of the claim. MPEP § 2143.

Claims 18, 19, and 22-27 depend from claim 17, and inherently contain the features of claim 17. Consequently, claims 18, 19, and 22-27 are allowable over the combination of Grisamore and Chang at least because any claim that depends from a nonobvious independent claim is also nonobvious.

Further regarding claim 18, the claim recites "the feedback input comprises one or more accumulator bits." The Office Action proposes that claim 18 is a method claim of claim 3 and is thus rejected for the same reasons as claim 3. See Office Action page 7. However, claim 3 recites that "the multiple input terms include one or more accumulator bits" as opposed to claim 18 which refers to a feedback input comprising accumulator bits. Consequently, claim 18 is not a method claim of claim 3 and so the reasons for the rejection of claim 3 are not applicable to claim 18. Further, the applicant does not find any teaching in Grisamore or Chang that could be equivalent to the recited feedback input, as recited in claim 18. For at least this additional reason, claim 18 is allowable over the combination of Grisamore and Chang.

Further regarding claim 25, the claim is rejected as follows: "[r]e claim 25, it is a method claim of claim 2. Thus, claim 25 is also rejected under the same rationale in the rejection of rejected claim 2." See Office Action page 8. However, claim 25 recites "the summing module generator comprises a multi-stage series of Boolean function generators incorporated in a dedicated logic device." This feature is not found anywhere in claim 2. Therefore, claim 25 could not be a method claim of claim 2, as the Office Action has proposed. The applicant does not find any teachings in the combination of Grisamore and Chang that could be considered equivalent to the recited features. For at least this additional reason, claim 25 is allowable over the combination of Grisamore and Chang.

The examiner rejects claims 13-16 and 28-31 under 35 U.S.C. § 103(a) as being unpatentable over Grisamore in view of Chang et al. as applied to claims 2 and 17 above, in further view of Fang et al. ("A Hierarchical Functional Structuring and Partitioning Approach for Multiple-FGPA Implementations"). The applicant traverses the rejections.

Claims 13-16 and 28-31 depend from claims 2 and 17, respectively, and inherently contain the features of these claims. Consequently, claims 13-16 and 28-31 are allowable over the combination of Grisamore, Chang, and Fang at least because any claim that depends from a nonobvious independent claim is also nonobvious.

Further regarding claim 13, the claim recites "inputs to couple the dedicated logic device with a controller." The Office Action has not identified any elements in Grisamore, Chang, or Fang that could be considered equivalent to the recited inputs and the applicant finds no such elements. Fang is merely cited for the proposition that a logic control module dynamically structures the atomic elements of a dedicated logic device and so does not remedy the deficiency of Grisamore and Chang. For at least this additional reason, claim 13 is allowable over the combination of Grisamore, Chang, and Fang.

Further regarding claim 16, "the logic control module dynamically structures the atomic elements of the dedicated logic device to implement desired instances of the architectural structure of the one or more full-adders, half-adders, and single registers." The Office Action has not pointed to any specific teachings of Grisamore, Chang, or Fang as being equivalent to these features and the applicant finds no such teachings. Specifically, even if Fang teaches that a logic control module dynamically structures the atomic elements of a dedicated logic device, as the Office Action proposes, it still does not teach desired instances of the architectural structure

of the one or more full adders, half adders, and single registers, as recited in the claim. For at least this additional reason, claim 16 is allowable over the combination of Grisamore, Chang, and Fang.

The examiner rejects claims 32, 36-38, and 42-43 under 35 U.S.C. § 103(a) as being unpatentable over Grisamore in view of Greenberger (U.S. Patent 6,411,979). The applicant traverses the rejections.

Regarding claim 32, the claim recites several features that are not taught in Grisamore as discussed above with respect to claims 2 and 44 including: associated registers, single registers, accumulator bits over a feedback path, and an integrated multi-input adder. Further, claim 32 recites "negating certain partial products and simultaneously passing the negated and non-negated partial products to a multi-stage series of Boolean function generators that implements one or more full-adders..." The Office Action acknowledges that Grisamore does not teach this feature, but proposes that Greenberger teaches this feature because it shows two different adders 34.1 and 34.2 in FIG. 2, one performing a subtraction and one performing an addition. However, claim 32 specifically refers to negating certain partial products and then passing all of the partial products to the adders. This is not what Greenberger teaches. Greenberger teaches that *signed digits* are passed to the adders 34.1 and 34.2, in which case negating the digits prior to passing them to the adders is not required. See Greenberger column 6, lines 3-12. Therefore, Greenberger does not teach negating certain partial products, and does not make up for the deficiency of Grisamore.

Grisamore also does not teach "passing the negated and non-negated partial products to a multi-stage series of Boolean function generators," as recited in claim 32. The Office Action did not address this feature of the claim in the rejection of claim 32. See Office Action page 10. However, in the rejection of claim 4, the Office Action acknowledges that Grisamore does not teach a plurality of Boolean function generators and relies on a combination with Chang to teach this feature. See Office Action page 6. Grisamore is not combined with Chang in the present rejection of claim 32 and since Greenberger does not teach a plurality of Boolean function generators, the combination of Grisamore and Greenberger also cannot teach this feature.

For at least the reasons identified above, claim 32 is allowable over the combination of Grisamore and Greenberger because the combination does not teach or suggest all of the features of the claim. MPEP § 2143.

Claims 36-38 and 42-43 depend from claim 32, and inherently contain the features of claim 32. Consequently, claims 36-38 and 42-43 are allowable over the combination of Grisamore and Greenberger at least because any claim that depends from a nonobvious independent claim is also nonobvious.

Further regarding claim 42, the claim recites "the multi-stage series of Boolean function generators are pipelined." As mentioned above with respect to claim 32, the combination of Grisamore and Greenberger does not teach Boolean function generators. Therefore, the combination cannot teach that Boolean function generators are pipelined, as recited in the claim. For at least this additional reason, claim 42 is allowable over the combination of Grisamore and Greenberger.

Further regarding claim 43, the claim recites "partitioning bits of equal significance into…single bits to be passed to single registers." As described above, with respect to claims 2 and 44, Grisamore does not teach single registers. Greenberger also does not teach single registers. Therefore, the combination of Grisamore and Greenberger cannot teach partitioning bits of equal significance and passing single bits to single registers, as recited in the claim. For at least this additional reason, claim 43 is allowable over the combination of Grisamore and Greenberger.

The examiner rejects claims 33-35 under 35 U.S.C. § 103(a) as being unpatentable over Grisamore in view of Greenberger a applied to claim 32 above, in further view of Chang et al. The applicant traverses the rejections.

Claims 33-35 depend from claim 32, and inherently contain the features of claim 32. Consequently, claims 33-35 are allowable over the combination of Grisamore, Greenberger, and Chang at least because any claim that depends from a nonobvious independent claim is also nonobvious.

The examiner rejects claims 39-41 under 35 U.S.C. § 103(a) as being unpatentable over Grisamore in view of Greenberger a applied to claim 32 above, in further view of Chang et al., as applied to claim 37 above, and in further view of Fang et al. The applicant traverses the rejections.

Claims 39-41 depend from claim 32, and inherently contain the features of claim 32. Consequently, claims 39-41 are allowable over the combination of Grisamore, Greenberger,

Chang, and Fang at least because any claim that depends from a nonobvious independent claim is also nonobvious.

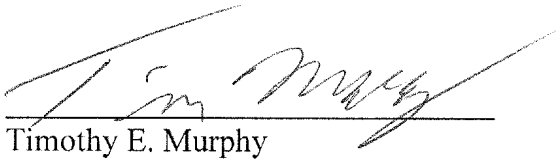
Conclusion

For the foregoing reasons, reconsideration and allowance of claims 2-5, 7-9, 11-19, and 22-49 of the application as amended is requested. The examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Timothy E. Murphy
Reg. No. 59,092

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613